REMARKS

This Amendment addresses the issues raised by the Examiner in the Office Action mailed June 7, 2004. Initially, Applicants would like to thank the Examiner for the careful consideration given this case. In view of the following remarks, Applicants feel that all outstanding issues have been addressed and prompt allowance of all remaining claims is respectfully requested.

Case Status

The parent case for this application issued as U.S. Patent No. 6,787,835 bearing a date of patent of September 7, 2004. The present continuation application was filed on March 2, 2004. A second preliminary amendment canceling Claims 1-17 and adding new Claims 18-34 was filed on June 4, 2004. The Examiner later issued an Office Action on June 7, 2004, but this Office Action did not take into account the second preliminary amendment filed on June 4th. Therefore, the Examiner's drawing and §112 rejection are not based on the claims that had been offered by Applicants in this case. The present response and amendment reintroduces Claims 18-34 form the June 4th preliminary amendment, and further addresses all of the Examiner's concerns.

Drawing Objection and 35 U.S.C. §112 Rejections

The Examiner indicated an objection to the drawings under 37 CFR 1.83(a) and a claim rejection based on 35 U.S.C. §112. Specifically, the drawings were objected to for failing to indicate a connection between the source or drain of the read transistor and one of the data lines, and a connection between the write transistor and the storage node. As indicated in the June 4th preliminary amendment, the claim amendment (now offered herein) overcome this objection by removing the objected-to language form the claims.

The Examiner's rejection of Claims 1-17 under §112 indicated that the claims were incomplete for omitting essential structural cooperative relationships of elements, "such omission amounting to a gap between the necessary structural connections. As with the drawing objection noted above, the claims as amended herein (and as amended prior to the Examiner's issuance of his June 7th Office Action) have been altered to overcome this rejection which was first posited in the parent case, now issued. As now written, the claims of the present application include all essential interconnection, and the claims are in condition for final allowance.

Comment on Prior Art References

Although no substantive rejection were submitted by the Examiner, Applicants would like to take this opportunity to comment on the differences between the present claims and the art that has previously been cited by the Examiner in this case and in the parent case. This discussion clearly shows that the present claims are in condition for final allowance, and prompt notice to such effect is respectfully requested.

In the parent application, the Examiner rejected claims over prior art including U.S. Patent No. 4,803,664 to Itoh ("Itoh"), U.S. Patent No. 5,492,851 to Ryou ("Ryou"), and U.S. Patent No. 5,977,591 to Fratin ("Fratin"). In the June 7th Office Action, the Examiner noted that U.S. Patent No. 5,646,903 to Johnson ("Johnson") is considered prior art. The present claims distinguish over all of this art.

Specifically, the Examiner in the parent case held that Itoh discloses all of the claimed subject matter except for the SOI thickness and then asserted that TFT transistors are well known and the film channel (57) would be obvious to one of skill in the art. However, the phenomenon of a low leakage current associated with a channel thickness below 5nm in a TFT structure was not heretofore known, and Itoh would not lead one to this invention. In fact, no other known entity has produced and used a 5nm channel, as a TFT is normally fabricated by doping impurities in the source or drain region in a polysilicon film with the same film thickness along the source to drain. If this conventional method is conducted in a very thin polysilicon film (as in the present invention), it is difficult to make contact with the source or drain. The present invention provides for ready contact with a "thickly" fabricated source or drain region with only the channel region being thinly formed (e.g., below 5nm).

Each of the independent claims includes a specific recitation of this distinguishing feature. Moreover, the claims have been amended herein to more clearly point out this feature. As such, each of the claims as amended herein distinguish over Itoh and are in condition for final allowance.

With respect to Fratin and Ryou, these references provide no additional teachings that, in combination with Itoh, render the present claims unpatentable. For example, the present invention as claimed includes two transistors in each memory cell (p-channel and n-channel) while Fratin uses a transistor including an n-type and p-type impurity into a single gate of a single transistor. Ryou utilizes a TFT as an upper level DRAM cell and a bulk silicon MOSFET as a lower DRAM cell, the upper cell formed on the lower cell with both cells performing the same function. The TFT on the upper cell has a large leakage current compared to the lower cell. The present invention, on the other hand, uses an extremely low

leakage current thin film TFT for charge storage and a MOSFET as a read transistor, the two transistors performing different functions, as claimed.

Further, the Johnson reference does not add any new arguments to those of the previously-utilized prior art. The invention proposed in Johnson is a specific structure for a memory cell composed of three conventional transistors in which the read and write data line is shared, the cell has separate read and write word lines, but the read word line of one cell is the same as the write word line of the neighboring cell. Johnson, therefore, purportedly achieves a reduction in memory cell size, but, when a row of cells is read, the adjacent row of cells has its data overwritten – an obviously large problem.

The present invention includes the use of a special transistor having a channel "which is formed by a semiconductor material with a thickness of no more than 5nm on top of an insulating film" (see e.g., Claim 18) for 2- and 3-transistor memory cells. The use of this special low-leakage transistor allows the memory cell to achieve a much longer retention time. Since this device is used to store the data charge on the storage node, the low-leakage leads to a long retention time (10-100x) and a much lower power memory than conventional transistors can offer (see ¶[119]). Various fabrication processes are proposed such that performance and memory cell size is further enhanced compared to conventional transistors. This results in 2- and 3-transistor memory cells with longer data retention (low power), relaxed fabrication methods, and small cell size.

Conclusion

The above claim amendments and accompanying remarks address each and every concern raised by the Examiner in the Office Action. Applicants believe that all remaining

claims of the present invention are now in condition for final allowance. If the Examiner feels that any issues remain outstanding, the Examiner is encouraged to contact Applicant's attorney at the contact information below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

Robert D. Kucler
Registration No. 45,908

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

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